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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/710,736	07/30/2004	Diane C. Boyd	FIS920040181US1	4735	
32074	32074 7590 05/05/2005			EXAMINER	
INTERNATIONAL BUSINESS MACHINES CORPORATION DEPT. 18G BLDG. 300-482 2070 ROUTE 52 HOPEWELL JUNCTION, NY 12533			OWENS, DOUGLAS W		
			ART UNIT	PAPER NUMBER	
			2811		
			DATE MAILED: 05/05/2005		

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
Office Action Summany	10/710,736	BOYD ET AL.				
Office Action Summary	Examiner	Art Unit				
	Douglas W. Owens	2811				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status _						
1) Responsive to communication(s) filed on	1) Responsive to communication(s) filed on					
2a) ☐ This action is FINAL . 2b) ☒ This	This action is FINAL . 2b)⊠ This action is non-final.					
3) Since this application is in condition for allowar	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is					
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4)⊠ Claim(s) <u>1-20</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1-10 and 20</u> is/are rejected.						
7) Claim(s) <u>11-19</u> is/are objected to.	•					
8) Claim(s) are subject to restriction and/or	8) Claim(s) are subject to restriction and/or election requirement.					
Application Papers						
9) The specification is objected to by the Examiner.						
10)⊠ The drawing(s) filed on <u>30 July 2004</u> is/are: a)⊠ accepted or b)⊡ objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119						
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 						
Attachment(s)						
 Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-948) 	4) Interview Summary (PTO-413) Paper No(s)/Mail Date					
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/30/04.		atent Application (PTO-152)				

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DETAILED ACTION

Claim Objections

Claims 1 – 19 are objected to because of the following informalities: line 13 of claim 1 recites the limitation, "the FET...". There is no antecedent basis for this limitation. Appropriate correction is required.

Claim Rejections - 35 USC § 112

- The following is a quotation of the second paragraph of 35 U.S.C. 112:
 The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
- 3. Claims 4 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 requires that an isolation trench be formed to separate the thinned SOI layer into first and second regions. The scope of the claim is vague, since it is not known if this a reference to the isolation trench mentioned in claim 1, or if this is an additional isolation trench.

Claim Rejections - 35 USC § 103

- 4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

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5. Claims 1, 2 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application Publication No. 2003/0170936 to Christensen et al. in view of US Patent Application Publication No. 2002/0060338 to Zhang.

Regarding claim 1, Christensen et al. teach a method of manufacturing a semiconductor device (Fig. 1, for example) comprising:

forming an SOI layer (Transistor layer) on a substrate;

forming an isolation trench separating the SOI layer into N and P ground regions (regions are identical to the claimed invention);

doping the N and P ground plane regions formed from the SOI layer with N-type and P-type dopants respectively (paragraph [0022]);

forming semiconductor channel regions above the N and P ground plane regions;

forming gate electrode stacks above the channel regions and the FET source and drain regions.

Christensen et al. do not teach a method including thinning the SOI layer to form an ultra-thin SOI layer. Zhang teach a method including thinning an SOI layer to form an ultra-thin SOI layer (paragraph [0005]). It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Zhang into Christensen et al., since it is desirable to reduce short channel effects.

With respect to the pre-amble language, It has been held that when the preamble merely states, for example, the purpose or intended use of the invention, rather than any distinct definition of any of the claimed invention's limitations, then the preamble is

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not considered a limitation and is of no significance to claim construction. *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1305, 51 USPQ2d 1161, 1165 (Fed. Cir. 1999). See also *Rowe v. Dror*, 112 F.3d 473, 478, 42 USPQ2d 1550, 1553 (Fed. Cir. 1997).

Regarding claim 2, Christenson et al. do not teach a method, wherein the SOI layer is thinned by successive oxidation and stripping steps. Zhang teaches a method, wherein the SOI layer is thinned by successive oxidation and stripping steps (paragraph [0005]). It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Zhang into the method taught by Christenson et al. for the reasons discussed above.

Regarding claim 20, Christenson et al. teach an FET (Fig. 1, for example), comprising:

an SOI layer on a substrate;

an isolation trench separating the SOI layer into N and P ground plane regions;

the N and P ground plane regions formed from the SOI layer doped with high doping levels of N-type and P-type dopant respectively;

semiconductor channel regions above the N and P ground plane regions;

FET source/drain regions juxtaposed with the channel regions; and
gate electrode stacks above the channel regions.

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Christensen et al. and Zhang as applied to claims 1 and 2 above, and further in view of US Patent Application Publication No. 2004/0256700 to Doris et al.

Christensen et al. and Zhang do not teach a method including forming a pad oxide and a pad nitride over the thinned SOI layer. Doris et al. teach forming a pad oxide (Fig. 4F; (51)) and a pad nitride (52). It would have been obvious to one of ordinary skill in the art to incorporate the method of Doris et al. into the proposed device of Christensen et al. and Zhang, since it is desirable to control etching of trench structures (Doris et al., paragraph [0066]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W. Owens whose telephone number is 571-272-1662. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Douglas W Owens Examiner

Dougle K. Owe

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